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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,426	08/10/2001	William A. Phillips	95-L-024C3 RE (1678-41)	6413

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STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
WELLS, KENNETH B	
ART UNIT	**PAPER NUMBER**
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/927,426	PHILLIPS ET AL.	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-12,16 and 17* is/are allowed.

6)☒ Claim(s) *1-6,13-15,18 and 20-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 5/11/07 has been received and entered in the case. The claims are objected to because they are not the proper format, i.e., insertions or deletions should be shown vis-à-vis the originally issued claims, see 37 CFR 1.173(b).

Specification

2. The disclosure is objected to because of the following informalities: In column 1 of the specification, line 4, after "This is a" the following should be inserted: --resissue of application serial no. 08/897,187 filed on 7/21/97 which is a--.

Appropriate correction is required.

Claim Objections

3. Claims 1, 9, 13, 24 and 30 are objected to because of the following informalities: in claim 1, on the second to last line, "to" should be changed to --from--. In claim 9, --a-- should be inserted at the end of the line. In claim 13, line 14, "and" (first occurrence) should be deleted. In claim 24, line 10, "are" should be changed to --is--. In claim 30, line 3, "A" should not be capitalized. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. Claims 1-18 and 20-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is misdescriptive, and therefore indefinite, to recite that each of the plural current mirror current sources and each of the plural current mirror current drains receive the same input signal (see lines 4-9). As shown in instant Fig. 5, the input signal received by FETs 82, 86, etc is not the same as the input signal received by FETs 84, 88, etc. It is also misdescriptive in claim 1 to recite that the currents through the plural current mirror current sources and the plural current mirror current drains are constant currents, because they are actually proportional to (and thus increase or decrease in response to) the input signal INPUT in instant Fig. 5. Note the same problem in claims 7, 13, 16-18, 21, 23, 29 and 32.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16, 18, 20, 21, 22, 26-28, 32, 34 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Huizer.

As to claim 18, note Fig. 3, where the recited "one current mirror current element" can be broadly interpreted to read on the combination FETs N2 and P22, because these two transistors together form a cascode-connected circuit, and a cascode circuit can be considered as "an element" (note also that FET P22 is shown as a current mirror transistor, i.e., its gate is tied to the gate of diode-connected FETs 1122 and 1126 shown in Fig. 5 of Huizer); the recited "enable input" of the cascode-connected element is at the source of FET P22 (i.e., where the enable signal Vdd is received); the recited "input" of the cascode-connected element is at the gate of FET N2 (i.e., where the recited input signal is received); the recited "constant current output" (to the extent each of applicant's FETs 82, 86, etc outputs a constant current) is the current which flows out from the cascode-connected element to the recited "fixed capacitor" 86b; the recited "programmable delay control circuit" reads on the combination of FET 96 and the unillustrated circuitry that outputs signal /C2; and the recited "output stage" (or "output circuit") reads on the next delay circuit stage in the series

(i.e., another Fig. 3 circuit that has a differential FET N1 or N2 that receives output signal 0 at the top plate of the fixed caspacitor 86b).

As to claim 21, note the analysis above with regard to claim 18. In addition, the recited "current circuit" and also the recited "current stage" of claim 21 can both be read on the circuit formed by the combination of FETs P22, N2, N52 and 91, either alone or in combination with the bias generating circuitry of Fig. 5; the recited "first and second levels" read on the low and high logic states of signal ib, respectively (or vice-versa, as per claim 26 which does not specifically recite which of the first and second levels is the logic high and which is the logic low); Finally, note that the recited first and third constant currents can be read on the currents that flowing through FET P22 at different times (the same is true for the recited second and fourth constant currents). Moreover, to the extent that these source and sink currents to/from capacitor 86b are equal at different times, claim 22 is anticipated as well (this will be the case when the amplitude of signal Vbp is stable).

As to claims 27 and 28, the first and/or second inverters are the next delay stage or next two delay stages in the chain (again, which are formed as shown in Figs. 3 and 5 of Huizer).

As to claim 32, note the above analysis with regard to claim 21.

As to claims 34 and 35, the recited delayed signal will inherently occur during operation of the Huizer delay circuitry, i.e., the delayed signal will be the output at terminal 0 (or any downstream output signal from a downstraem stage). Note also that in claim 34 the recited first and third levels can be equal to each other, and the same is true for the recited second and fourth levels.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 13-15, 23, 24 and 29-31 rejected under 35 U.S.C. 103(a) as being unpatentable over any one of Yousefi-Elezi, Chen and Furutani in view of Huizer.

As to claims 23 and 29, each of the above-noted primary references discloses the use of delay elements with their delay

time being responsive to both source and sink mirror currents. Not disclosed is that each of the mirror currents is adjustable responsive to plural enable signals provided by a control circuit which outputs plural enable signals to plural current source/sink stages. Such would have been obvious, however, to any person having ordinary skill in the art in view of the above-noted teachings of Huizer. The motivation such such a modification is to provide improved delay control of the delay signals circulating through the delay chains in the primary references (e.g., better resolution/finer adjustment of the phase shift, improved ability to keep the input/output signals in synchronization with each other, etc).

As to claim 24, note the above analysis with regard to claim 22.

As to claims 30 and 31, the recited "current generator" reads on FET P22, N52 and 91 together with the bias generating circuitry of Fig. 5.

As to claims 1, 2 and 13-15, these claims will also be met by the above-noted combination of references if the "plurality of current mirror sources (or elements)" are interpreted as the combination of FETs P22 and N2 (a first current mirror source) and the combination of FETs P21 and N2 (a second current mirror source), and the plural adjustable current mirror transistor

teaching of Huizer is also used to form plural current drain stages in each of the above-noted primary references.

As to claims 3-6, the details of the programming to from the enable signals also would have been obvious because these are all well-known (typical in the art) ways of programming control digital signals, of which fact official notice is taken by the examiner.

7. Claims 25 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huizer.

Maintaining the source and sink currents to/from capacitor 86b equal, though not disclosed by Huizer, nevertheless would have been obvious to any person having ordinary skill in the art who will easily recognize that such a relationship between the source and sink currents needs to exist to keep a symmetrical and/or 50% duty cycle signal circulating through the delay chain in Fig. 1 of Huizer.

Allowable Subject Matter

8. Claims 7-12, 16 and 17 are allowed.

Claims 7 and 17 are allowable in view of the details of the input stage, i.e., first and second input transistors which receive the input signal, first and second bias transistors and

a resistor between bias transistors. No motivation is seen for such an input stage in any of the prior art of record. Claim 16 is allowable in view of the limitations on lines 16-19 thereof.

Conclusion

9. In view of the above-noted new grounds of rejection not necessitated by applicant's amendments, this office action is non-final.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew N. Richards, can be reached at (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is (571)273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kenneth B. Wells/
Primary Examiner
Art Unit 2816

September 26, 2007